AMENDMENTS TO THE CLAIMS

1. (Currently Amended): A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising:

forming an amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a gate electrode on the amorphous silicon layer;

doping impurities of a first conductive type in the amorphous silicon layer;

forming a metal layer on exposed portions of the amorphous silicon layer; and

crystallizing the amorphous silicon layer by applying thermal treatment and an electric field to the resultant substrate,

wherein the thin film transistor includes source and drain regions and a channel region, and wherein the amorphous silicon layers in the source and drain regions are crystallized by MIC and the amorphous silicon layer in the channel region is crystallized by FALC during the application of the thermal treatment and electric field, whereby the amorphous silicon layer in the channel region is substantially free from metal atoms of the metal layer ~~having crystallized amorphous silicon layer is formed at each of the plurality of pixels, and wherein a low off current of about 3.72×10^{-13} A to about 6.5×10^{-11} A is obtained~~.

2. (Previously Presented): The method of fabricating a thin film transistor according to claim 1, wherein the substrate includes a material selected from the group consisting of a glass and a glass having an oxide layer formed thereon.

3. (Previously Presented): The method of fabricating a thin film transistor according to

claim 1, wherein the substrate includes a material selected from the group consisting of a silicon wafer and a silicon wafer having an oxide layer formed thereon.

4. (Previously Presented): The method of fabricating a thin film transistor according to claim 1, wherein the gate electrode is formed by at least one transition metal selected from the group consisting of Mo, Cr and Co.

5. (Previously Presented): The method of fabricating a thin film transistor according to claim 1, wherein the impurities include PH_3.

6. (Original): The method of fabricating a thin film transistor according to claim 1, wherein the metal layer has a thickness of no more than 30Å.

7. (Previously Presented): The method of fabricating a thin film transistor according to claim 6, wherein the metal layer is formed by at least one transition metal selected from the group consisting of Cu, Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Se, Ti, V, Cr, Mn, Zn, Au and Ag.

8. (Previously Presented): The method of fabricating a thin film transistor according to claim 1, wherein the step of forming metal layers on exposed portions of the amorphous silicon layer is performed before the step of doping impurities of first conductive type in exposed portions of the amorphous silicon layer.

9. (Original): The method of fabricating a thin film transistor according to claim 1, further comprising a step of forming electrodes for applying a voltage to form the electric field

on the resultant substrate.

10. (Previously Presented): The method of fabricating a thin film transistor according to claim 9, wherein the electrodes are formed by a metal selected from the group consisting of Au, Pt, Fe and Al.

11. (Previously Presented): The method of fabricating a thin film transistor according to claim 9, wherein at least a first electrode and a second electrode are formed prior to the crystallizing step, and crystallization of the amorphous silicon layer occurs faster at the first electrode than at the second electrode.

12. (Previously Presented): The method of fabricating a thin film transistor according to claim 9, wherein at least a negative electrode and a positive electrode are formed prior to the crystallizing step, and crystallization of the amorphous silicon layer occurs faster at the negative electrode than at the positive electrode.

13. (Original): The method of fabricating a thin film transistor according to claim 1, where the heat treatment is performed at about 500°C.

14. (Currently Amended): A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising:

forming a first amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a second amorphous silicon layer as a gate electrode on the first amorphous silicon layer;

doping impurities of a first conductive type in the first and second amorphous silicon layers;

forming a metal layer on doped portions of the first and second amorphous silicon layers; and

crystallizing the first and second amorphous silicon layers by performing heat treatment and applying an electric field on the resultant substrate,

wherein the thin film transistor includes source and drain regions and a channel region, and wherein the first amorphous silicon layers in the source and drain regions are crystallized by MIC and the first amorphous silicon layer in the channel region is crystallized by FALC during the application of the thermal treatment and electric field, whereby the first amorphous silicon layer in the channel region is substantially free from metal atoms of the metal layer ~~having crystallized amorphous silicon layer is formed at each of the plurality of pixels, and wherein a low-off current of about 3.72×10^{-13} A to about 6.5×10^{-11} A is obtained~~.

15. (Original): The method of fabricating a thin film transistor according to claim 14, wherein the substrate includes one of a glass and an oxide layer on a glass.

16. (Original): The method of fabricating a thin film transistor according to claim 14, wherein the substrate is prepared by depositing an oxide layer on a silicon wafer.

17. (Original): The method of fabricating a thin film transistor according to claim 14, wherein the step of forming the gate insulating layer and the second amorphous silicon layer comprises the steps of:

depositing an oxide layer and an amorphous silicon layer on the substrate comprising the

first amorphous silicon layer;

etching the oxide layer and the amorphous silicon layer using a mask for forming the gate electrode.

18. (Original): The method of fabricating a thin film transistor according to claim 14, wherein the impurities include p-type or n-type.

19. (Original): The method of fabricating a thin film transistor according to claim 14, wherein the metal layer has a thickness of no more than 30 Å.

20. (Original): The method of fabricating a thin film transistor according to claim 14, the step of forming metal layers on the doped portions of the amorphous silicon layer is performed before the step of doping impurities of first conductive type in exposed portions of the first and second amorphous silicon layers.

21. (Previously Presented): The method of fabricating a thin film transistor according to claim 14, further comprising a step of forming electrodes for applying a voltage to form the electric field on the resultant substrate.

22. (Original): The method of fabricating a thin film transistor according to claim 21, wherein the electrodes are formed by a metal material including Au, Pt, Fe and Al.

23. (Previously Presented): The method of fabricating a thin film transistor according to claim 21, wherein at least a first electrode and a second electrode are formed, and crystallization

of the amorphous silicon layer occurs faster at the first electrode than at the second electrode.

24. (Original): The method of fabricating a thin film transistor according to claim 21, wherein the electrodes includes a negative electrode and a positive electrode, and crystallization of the amorphous silicon layer occurs faster at the negative electrode than at the positive electrode.

25. (Currently Amended): A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising:

forming an amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a gate electrode on the amorphous silicon layer;

forming a metal layer on exposed portions of the amorphous silicon layer;

doping impurities of a first conductive type in the amorphous silicon layer after the metal layer is formed; and

crystallizing the amorphous silicon layer by applying thermal treatment and an electric field to the resultant substrate,

wherein the thin film transistor includes source and drain regions and a channel region, and wherein the amorphous silicon layers in the source and drain regions are crystallized by MIC and the amorphous silicon layer in the channel region is crystallized by FALC during the application of the thermal treatment and electric field, whereby the amorphous silicon layer in the channel region is substantially free from metal atoms of the metal layer ~~having crystallized amorphous silicon layer is formed at each of the plurality of pixels and wherein a low off current of about 3.72×10^{-13} A to about 6.5×10^{-11} A is obtained~~.

26. (Previously Presented): The method of fabricating a thin film transistor according to claim 25, wherein the substrate includes a material selected from the group consisting of a glass and a glass having an oxide layer formed thereon.

27. (Previously Presented): The method of fabricating a thin film transistor according to claim 25, wherein the substrate includes a material selected from the group consisting of a silicon wafer and a silicon wafer having an oxide layer formed thereon.

28. (Previously Presented): The method of fabricating a thin film transistor according to claim 25, wherein the gate electrode is formed by at least one transition metal selected from the group consisting of Mo, Cr and Co.

29. (Previously Presented): The method of fabricating a thin film transistor according to claim 25, wherein the impurities include PH_3.

30. (Previously Presented): The method of fabricating a thin film transistor according to claim 25, wherein the metal layer has a thickness of no more than 30Å.

31. (Previously Presented): The method of fabricating a thin film transistor according to claim 30, wherein the metal layer is formed by at least one transition metal selected from the group consisting of Cu, Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Se, Ti, V, Cr, Mn, Zn, Au and Ag.

32. (Previously Presented): The method of fabricating a thin film transistor according to claim 25, wherein the heat treatment is performed at about 500°C.

33. (Previously Presented): The method of fabricating a thin film transistor according to claim 25, further comprising a step of forming electrodes for applying a voltage to form the electric field on the resultant substrate.

34. (Previously Presented): The method of fabricating a thin film transistor according to claim 33, wherein the electrodes are formed by a metal selected from the group consisting of Au, Pt, Fe and Al.

35. (Previously Presented): The method of fabricating a thin film transistor according to claim 33, wherein at least a first electrode and a second electrode are formed prior to the crystallizing step, and crystallization of the amorphous silicon layer occurs faster at the first electrode than at the second electrode.

36. (Previously Presented): The method of fabricating a thin film transistor according to claim 33, wherein at least a negative electrode and a positive electrode are formed prior to the crystallizing step, and crystallization of the amorphous silicon layer occurs faster at the negative electrode than at the positive electrode.

37. (Currently Amended): A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising:

forming an amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a gate electrode on the amorphous silicon layer;

doping impurities of a first conductive type in the amorphous silicon layer;

forming a metal layer on exposed portions of the amorphous silicon layer; and

crystallizing the amorphous silicon layer by applying thermal treatment and an electric field to the resultant substrate,

wherein the thin film transistor includes source and drain regions and a channel region, and wherein the amorphous silicon layers in the source and drain regions are crystallized by MIC and the amorphous silicon layer in the channel region is crystallized by FALC during the application of the thermal treatment and electric field, whereby the amorphous silicon layer in the channel region is substantially free from metal atoms of the metal layer ~~having crystallized amorphous silicon layer is formed at each of the plurality of pixels minimizing metallic contamination in the channel region during crystallization and wherein a low off current of about 3.72×10^{-13} A to about 6.5×10^{-11} A is obtained~~.